

REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested.

Claims 1-5 and 7-17 are currently pending.

Claim Rejections - 35 USC § 103

Claims 1 and 2 were rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Wada et al. (U.S. Patent No. 6,225,846, hereinafter "Wada") in view of Fujita et al. (U.S. Patent No. 6,215,159, hereinafter "Fujita").

Claims 3-10 were rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Wada in view of Fujita and further in view of Rossi et al. (U.S. Patent No. 6,069,513, hereinafter "Rossi").

Claims 11-17 were rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Wada and Fujita in view of Rossi and further in view of Gillingham et al. (U.S. Patent No. 6,510,503, hereinafter "Gillingham").

In the Amendment filed June 25, 2004 with the Request for Continued Examination, Applicants amended the claims to recite structure that provides the dynamic repeater a noise margin of about  $V_{cc}/2$ , which is achieved by balancing the circuit such that an input voltage of  $V_{cc}/2$  produces an output voltage of  $V_{cc}/2$  in the evaluate mode.

Consider exemplary independent claim 1, which recites in relevant part:

"...a plurality of transistors coupled between the input transistor and the output node,

wherein the input transistor and said plurality of transistors are sized in a ratio such that the output node is operative to

output a voltage of  $V_{cc}/2$  in response to a voltage of  $V_{cc}/2$  on the input node in the evaluate mode."

The present Action does not address the structural or noise margin limitations. Accordingly, Applicants submit that the Action has failed to make a prima facie case of obviousness.

None of Wada, Fujita, Rossi, and Gillingham teaches or suggests, either alone or in combination, a dynamic bus repeater with a noise margin of  $V_{cc}/2$  or a balanced circuit that produces an output voltage of  $V_{cc}/2$  in response to an input voltage of  $V_{cc}/2$  in the evaluate mode. Accordingly, Applicants submit that independent claims 1 and 11 and their dependencies are allowable.

#### Conclusion


It is believed that all of the pending claims have been addressed in this paper. However, failure to address a specific rejection, issue, or comment, does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above are not intended to be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Claims 1-5 and 7-17 are in condition for allowance, and a notice to that effect is respectfully solicited. If the Examiner has any questions regarding this response, the Examiner is invited to telephone the undersigned at (858) 678-4321.

Please apply any charges or credits to deposit  
account 06-1050.

Respectfully submitted,

Date: December 21, 2004

  
\_\_\_\_\_  
Scott C. Harris  
Reg. No. 32,030

Attorneys for Intel Corporation  
**PTO Customer No. 20985**  
Fish & Richardson P.C.  
12390 El Camino Real  
San Diego, California 92130  
Telephone: (858) 678-5070  
Facsimile: (858) 678-5099

/BY  
**KENYON S. JENCKES**  
**REG. NO. 41,873**

10467950.doc